L Number	Hits	Search Text	DB	Time stamp
-	71133	boot$up boot$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:13
-	3507	boot$up boot$4 and mother$board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:13
-	2354	boot$up boot$4 and mother$board and (daughter$board)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:14
-	2354	boot$up boot$4 and mother$board and (daughter$board sister$board)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:13
-	2354	boot$up boot$4 and mother$board and (daughter$board brother$board)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:13
-	2324	boot$up boot$4 and mother$board and daughter$board and mother$board with stor$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:15
-	2322	boot$up boot$4 and mother$board and daughter$board and mother$board with stor$4 with device	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:15
-	2319	boot$up boot$4 and mother$board and daughter$board and mother$board with stor$4 with device and daughter$board with boot$4 with (code instruction program)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:16
-	2319	boot$up boot$4 and mother$board and daughter$board and mother$board with stor$4 with device and daughter$board with boot$4 with (code instruction program) and (coupler (coupling near2 device))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:16
-	2319	boot$up boot$4 and mother$board and daughter$board and mother$board with stor$4 with device and daughter$board with boot$4 with (code instruction program) and (coupler (coupling near2 device)) and coupl$4 with daughter$board with mother$board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:17
-	2319	boot$up boot$4 and mother$board and daughter$board and mother$board with stor$4 with device and daughter$board with boot$4 with (code instruction program) and (coupler (coupling near2 device)) and coupl$4 with daughter$board with mother$board and kiiir	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:17
-	0	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 with device and daughter$board with boot$4 with (code instruction program) and (coupler (coupling near2 device)) and coupl$4 with daughter$board with mother$board and kiiir	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:19
-	0	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 with device and daughter$board with boot$4 with (code instruction program) and (coupler (coupling near2 device)) and coupl$4 with daughter$board with mother$board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:18

-	52	(boot$up boot$4) and mother$board and daughter$board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:18
-	0	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 and daughter$board with boot$4 with (code instruction program)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:19
-	1	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 and daughter$board with (code instruction program) and (coupler coupling)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:31
-	2	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 and daughter$board with (code instruction program)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:31
-	2	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 and daughter$board with (code instruction program) and (coupler coupl$4)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/08/27 13:31
-	14	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 13:52
-	0	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 and emulat$4 and emulator	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 13:52
-	9	(boot$up boot$4) and mother$board and daughter$board and mother$board with stor$4 and emulat$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 13:55
-	77	(boot$up boot$4) and mother$board and mother$board with stor$4 and emulat$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 13:55
-	68	(boot$up boot$4) and mother$board and mother$board with stor$4 and emulat$4 and port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 13:56
-	6	(boot$up boot$4) and mother$board and mother$board with stor$4 and emulat$4 and port and port with emulat$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 13:59
-	20	(boot$up boot$4) and mother$board and emulat$4 and port and port with emulat$4 and receiv$4 with emulat$4	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 14:00
-	17	(boot$up boot$4) and mother$board and emulat$4 and port and port with emulat$4 and receiv$4 with emulat$4 and emulator	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 14:00
-	17	(boot$up boot$4) and mother$board and emulat$4 and port and port with emulat$4 and receiv$4 with emulat$4 and emulat$4 with device	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 14:24
-	19	(boot$up boot$4) and mother$board and emulat$4 and port and port with emulat$4 and (send$4 transmit$4 receiv$4) with emulat$4 and emulat$4 with device	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 14:35
-	1	(boot$up boot$4) and mother$board and emulat$4 and port and port with emulat$4 and (send$4 transmit$4 receiv$4) with emulat$4 and emulat$4 with device and development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 14:26

-	19	(boot$up boot$4) and mother$board and emulat$4 and port and port with emulat$4 and (send$4 transmit$4 receiv$4) with emulat$4 and emulat$4 with device and emulat$4 with (connect$4 coupl$4)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/01/09 14:36
-	123327	printed adj circuit adj board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:20
-	2178	printed adj circuit adj board with processor	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:19
-	0	printed adj circuit adj board with processor and processor with development adj port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:21
-	338	printed adj circuit adj board with processor and processor with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:20
-	58	printed adj circuit adj board with processor and processor with port and bus with process$4 with board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:20
-	7	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and bus with board with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:39
-	0	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and bus with board with port and first adj boar and second adj board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:38
-	58	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and bus	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:39
-	0	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and first adj board and second adj board and coupler	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:40
-	2	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and first adj board and second adj board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:55
-	1465	printed adj circuit adj board with motherboard	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:56
-	79	printed adj circuit adj board with motherboard with daughterboard	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/24 14:56
-	0	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:19
-	10	printed adj circuit adj board with processor and development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:22
-	0	printed adj circuit adj board with processor and processor with port and bus with process$4 with board and development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:21
-	8	printed adj circuit adj board with processor and processor with port and development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:22

-	0	printed adj circuit adj board with processor and processor with port and process$4 with development adj port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:21
-	0	printed adj circuit adj board with processor and development adj port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:22
-	7	printed adj circuit adj board with processor and processor with development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/26 15:22
-	7	printed adj circuit adj board with processor and processor with port and processor with development with port	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 08:26
-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and first adj board and second adj board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 08:27
-	5	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 08:27
-	5	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 09:39
-	5	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 09:47
-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with board with processor	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 09:47
-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 09:47
-	5	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 09:56
-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and second near4 board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 09:53
-	5	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 10:05

-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and stor$4 with board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 10:06
-	2	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and stor$4 same board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 10:07
-	2	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 10:23
-	2	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board and board with (link$4 communicat$4 connect$4 path)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 11:51
-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board and board with (link$4 communicat$4 connect$4 path) and dram with bus	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 11:53
-	2	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board and board with (link$4 communicat$4 connect$4 path) and dram samebus	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 11:53
-	0	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board and board with (link$4 communicat$4 connect$4 path) and dram same bus	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 11:53

-	2	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board and board with (link$4 communicat$4 connect$4 path) and dram	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 11:59
-	2	printed adj circuit adj board with processor and processor with port and processor with development with port and (multiple plural$4) with boards and (multiple plural$4) with bus and processor with board and bus with processor and printed adj circuit adj board and (memory stor$4) same board and board with (link$4 communicat$4 connect$4 path) and dram and serial with bus	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/05/27 11:59